Testing and fault tolerance of integrated circuits

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Abstract. Today, the technological advances reduce the size of electronic components to the nanometer dimensions. This miniaturization makes manufacturing processes more complex and less reliable. This implies that it becomes very difficult to manufacture a circuit without any defects. Therefore, the manufacturing yield could decline significantly. To improve yield, fault-tolerant structures could be used in the future, with the objective to tolerate manufacturing defects to make more circuits operating. However, the higher expectation of reliability can only be met by more thorough and comprehensive testing of this structure. This paper analyzes the ability of these structures to tolerate manufacturing defects and the conditions to improve the yield. It is also shown that with the help of partitioning techniques the tolerance of TMR structures can be improved and therefore their reliability and manufacturing yield.

Keywords: test, yield, reliability, fault tolerance, Design for reliability, design for test.

1 INTRODUCTION

Since the advent of microelectronics in the 1960s, this area has continued to grow, both in science and research as in everyday life with personal computers and mobile phones. Since 2010, the resolution of integrated circuits increased to 22 nm [ITRS, (2007)]. This miniaturization of manufacturing processes and increasing the number of interconnect levels have helped integrate real systems on a chip. Current systems integrate more and more heterogeneous functional blocks (digital, analog, memory, RF, MEMS, etc ...). However, if the early integration of circuits had intended only to integrate more functions in the least possible surface, today's research performance becomes a strategic argument. Indeed, with the advent of submicron technologies heavily, some physical phenomena that were previously negligible become dominant and these phenomena can induce failures and have a direct impact on the reliability and manufacturing yield. This implies that it becomes very difficult to manufacture a circuit without any defects. Therefore, testing of integrated circuits has become an essential task in the semiconductor industry.

The motivation of our work is to propose robust structural solutions included in the design flow of integrated circuits that improve and ensure reliability even in the presence of defects. The proposed methodology consists of two approaches: technical testing of circuits in order to detect their failures by using the ATPG (Automatic Test Pattern Generator) and fault tolerance technique by using the TMR (Triple Modular Redundancy) structure. This methodology is applied to combinational circuits of ISCAS85 and ITC99 benchmarks modified into TMR structures. The tests show that, although the reliability is improved, the TMR structures are not fault-tolerant enough to offset their cost in silicon area. We propose to optimize these structures by increasing their redundancy by the method of partitioning. The results show that partitioning greatly improves the fault tolerance of the majority of circuits

tested and therefore their reliability and the manufacturing yield. This paper show that the manufacturing yield, and consequently the reliability depend on the cost in silicon area and consumption.

2 TEST OF INTEGRATED CIRCUITS

The advent of integrated circuit technology has introduced electronics in many aspect of present-day life. As the use of electronic components increases, the expectation of lower cost, better accuracy, and higher reliability increases. Lower cost and better accuracy is achieved by putting more transistors per unit of silicon, using design automation, increasing device operation speed, and reducing its power consumption. However, these design steps cannot guarantee reliability. In fact, as the circuit density increases, the probability of a manufacturing defect increases. The higher expectation of reliability can only be met by more thorough and comprehensive testing. Classical fault models (stuck-at, stuck-open, stuckon …) have been proved to be efficient for the analysis of many of these faults and the majority of the techniques of test are based on these models of faults (Cimino, 2007; Machouat, 2008). However, it is well-known that these fault models cover only partially the spectrum of real failures in today's integrated circuits and the functional test tends to being replaced by the structural test (Cimino, 2007; Machouat, 2008; Bounceur, 2007).

The effectiveness of the test depends on the Y (Yield), the FC (Fault Coverage) and the DL (Defect Level) respectively corresponding to the ratio of the number of circuits that pass the test on the total number of circuits, the ratio of the number of faults detected on the total number of errors and report the number of circuits on the number of faulty circuits that pass the test. As in (1), studies (Bounceur, 2007) showed that:

$$DL = [1- Y^{(1-FC)}] \times 100\ \% \quad , \qquad (1)$$

3 DESIGN FOR RELIABILITY AND FAULT TOLERANCE

The concept of fault tolerance refers to a method of designing a circuit that allows it to continue functioning even in the presence of faults. From the point of view of technology, there are several faults tolerance structures (Han and Jonker, 2005; Hafezparast, 1990). These structures have been designed to tolerate transient or temporary faults but they can also tolerate manufacturing defects and thus increase the yield. They all use the concept of redundancy of which the principle is to use material resources to correct the faults. We chose to use the well-known example, which is the TMR (Triple Modular Redundancy) structure shown in Fig.1. In TMR structure the circuit is established three times. The outputs of these three identical circuits are voted by a majority voter for to give an output single. The reliability of TMR structure is given by solving the following equation (2) (Hafezparast, 1990):

$$R_{TMR}(t) = R_{Voter} \times \sum_{i=2}^{3} (C_3^i \times R(t)^i\,[1 - R(t)]^{3-i}), \qquad (2)$$

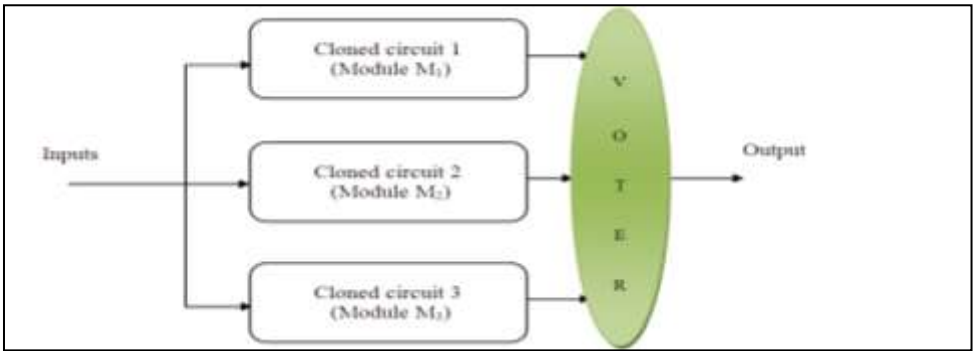

Fig. 1. TMR structure.

However, the technical realization of such structures is very expensive. Therefore the motivations of designers are not making so many designs for reliability with the manufacturing yield the highest possible, but to determine the manufacturing process that aims to develop reliable circuits with a production cost of the lowest possible.

3.1 Calcul of manufacturing yield of TMR structure

Considering that A_C the original surface of the circuit without redundancy and A_V the surface of the voter. If we neglect the size of the interconnections, the TMR structure surface A_{TMR} is given by (3) ((Stapper, 1984; Siewiorek and Swarz, 1992) :

$$A_{TMR} = 3\,A_C + A_V \qquad (3)$$

The area cost A_O (Area Overhead) of the implementation of a circuit structure transformed into TMR is then:

$$A_O = \frac{3\,A_C + AV}{A_C} = 3 + \frac{A_V}{A_C}$$

By calling Y_{TMR} the manufacturing yield of the TMR structure and Y_C the manufacturing yield of the structure without redundancy, the condition so that TMR structure increases the yield and therefore the reliability is as follows: $Y_{TMR} > A_O \times Y_C$. Like $Y_{TMR} \leq 1$, this condition becomes: $Y_C \leq 1/Ao$

4 APPLICATION

In our application we have used combinational circuits of benchmarks ISCAS85 and ITC99 (Web site). Next, we transformed their architecture into TMR structure. For an effective test of TMR, a new fault models should be introduced into the ATPG, allowing detection of several manufacturing faults. Furthermore, for to see the behavioral of circuit in the presence multiple simultaneous faults, we have injected of pairs of stuck- at faults (s@0, s@1) for verifying tesatability at the verilog level. The ATPG gives us the FC (Fault Coverage) rate, and T: tolerance probability, that a pair of faults either tolerated by the structure, defined by: T = number of pairs of faults tolerated / total number of pairs of faults. To calculate the probability T, we used the simulation software Tetramax (Web sit). Table 1 summarizes the characteristics of the circuits tested.

Table 1. Characteristics of the circuits tested.

simulated circuit		In/Out	Number of Gates	Number of Stuck-at faults	Number of pairs of Faults	Pairs of faults reduced by ATPG	A_O (%)	T (%)	R (%)
Benchmarks ISCAS85	c432	36/7	160	392	689725	75.10^3	3.10	40,00	35,2
	c499	41/32	202	486	1062153	95.10^3	3.39	52,73	54,09
	c1908	33/25	880	1826	15001503	$1.3.10^6$	3.08	56,45	59,62
	c2670	233/140	1193	2852	36598290	$1.87.10^6$	3.33	75,96	85,44
	c3540	50/22	1669	3438	53184141	$4.91.\ 10^6$	3.04	54,09	56,12
	c5315	178/123	2307	4970	111146595	$3.4.\ 10^6$	3.16	93,20	98,67
	c6288	32/32	2416	6250	175771875	$18.2.10^6$	3.03	38,03	32,38
	c7552	207/108	3512	7438	248946141	$7.40.\ 10^6$	3.09	84,93	93,87
Benchmarks ITC99	b02	1/1	25	64	18336	$1.5.\ 10^3$	3.47	86,37	94,93
	b03	4/4	150	382	656085	$290.\ 10^3$	3.57	87,93	95,98
	b04	11/8	480	1477	9814665	$535.\ 10^3$	3.32	84,30	93,37
	b05	1/36	608	2553	29326311	$1.17.10^6$	3.16	88,66	96,43
	b06	2/6	66	155	107880	$7.73.10^3$	3.68	87,50	95,70
	b07	1/8	382	1120	5643120	$399.\ 10^3$	3.38	81,90	91,35
	b09	1/1	131	417	781875	$57.3.\ 10^3$	3.45	83,07	92,37
	b10	11/6	172	468	984906	$63.5.\ 10^3$	3.31	89,40	96,86
	b11	7/6	366	1308	7696926	$703.\ 10^3$	3.19	74,50	83,80
	b12	5/6	1000	2777	34698615	$857.\ 10^3$	3.30	95,46	99,40
	b13	10/10	309	835	3136260	$59.6.\ 10^3$	3.49	96,96	99,72

4.1 Impact of cost in silicon area on tolerance probability T

Figure 2 show that the transformation of circuits in TMR structures does not increase their manufacturing yield, and thus their reliability. The cost in silicon area due to their achievement is very high and tolerance is not enough to offset. In other words, for that realization of TMR structures will lead to increased performance of a circuit, the circuits must be above the curve (T>Tmin) which is not the case in Fig.2.

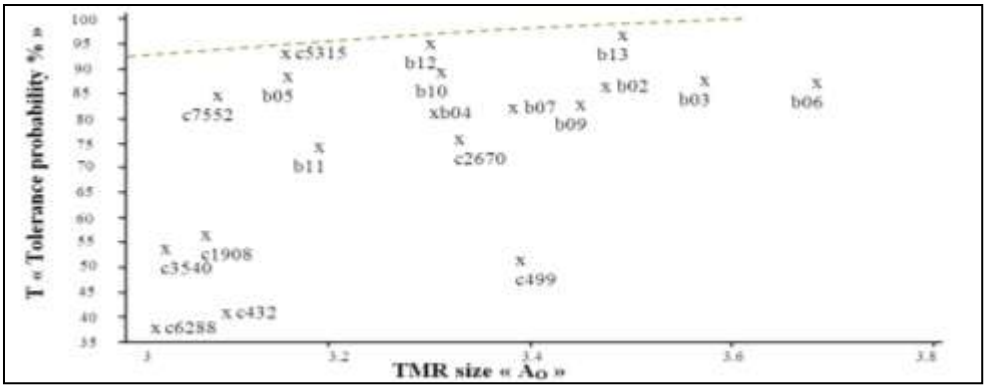

Fig. 2. Faults tolerance of circuits depending on the cost (A_O).

4.2 Optimization of tolerance probability of TMR

Consequently, for that TMR structures can increase reliability through increased manufacturing yield, other solutions must be found. Two possible ideas are needed: either to reduce the cost in silicon area, in other words, to use another type of structure, or to use one of the design methods of partitioning to reinforce the redundancy of TMR structures (Edmond Bichot, 2007). It is this second solution which we chose to implement. Partitioning has two positive effects on faults tolerance. First, it reduces the combinatorial depth of circuits, which reduces the number of paths of errors propagation. Second, it makes each partition independently. Thus, a manufacturing defect in a part of the partition has no impact on another part of the partitioning. TMR structure is modified by partitioning each channel into two or three partitions. A voter is placed between each partition. The Fig. 3 shows the three structures TMR Simple, TMR Double and TMR Triple.

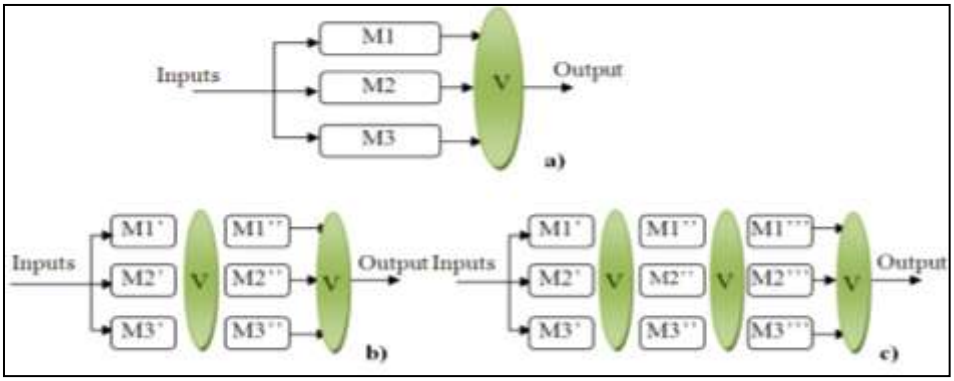

Fig. 3. TMR structure partitioning a) TMR Simple b) TMR Double c) TMR Triple.

From figure 4, it is clear that with the help of partitioning techniques the tolerance of TMR structures can be improved and the majority of circuits tested have their characteristics ranging between the curves corresponding to the two cases: voter not robust and voter robust. However, if the design effort is made to make the strongest possible voters, the real curve Tmin corresponding to these efforts would be between the two extreme cases presented in Fig.4 (robut and not robust voter).

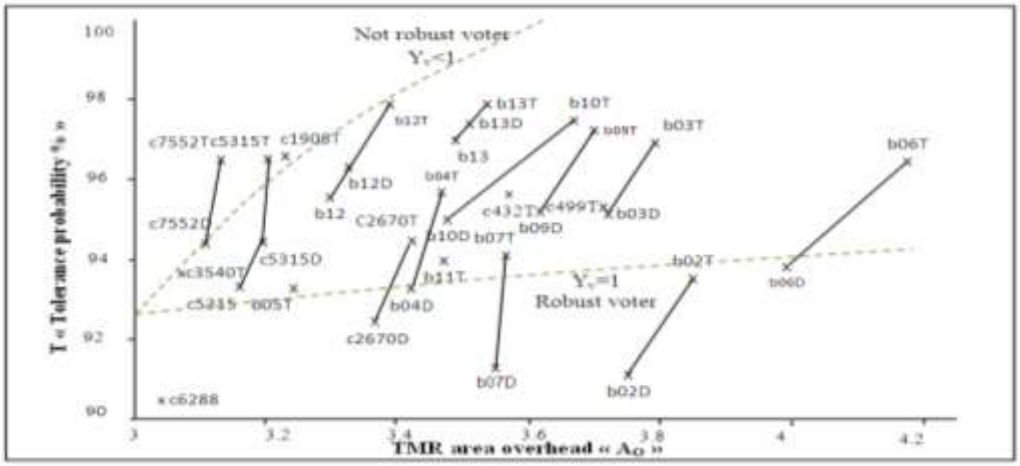

Fig. 4. TMR structure partitioning a) TMR Simple b) TMR Double c) TMR Triple.

Table 2 summarizes the characteristics of TMR structures partitioned. We find that the area overhead of partitioning of TMR structure is lower for larger circuits. Indeed, less than 2% for the largest ISCAS85 circuits and less than 5% for the largest ITC99 circuits. This low area overhead is a positive point for the Tmin probability which can thus satisfy the condition T > Tmin required. Indeed several structures, in particular TMR triple satisfied the conditions for increasing the reliability and manufacturing yield. The symbol NA (not applicable boxes marked) means that the area cost is very high, even if 100% of pairs of faults were tolerated. For example, for the circuit b06, whatever the mathematical law of distribution of defects, increase reliability and performance will never be possible with TMR structures.

Table 2: Partitioning results

Simulated circuit	**Simple TMR**	**Double TMR**		**Triple TMR**						
							Robusts voters		**Not robusts voters**	
	Voters number	Voters number	A_O (%)	Voters number	A_O (%)	T (%)	T_{min} (%)	R (%)	T_{min} (%)	R (%)
c432	7	29	10.55	38	14.86	95,53	93,59	99,41	99,61	88,48
c499	32	49	6.14	59	9.75	95,11	93,79	99,30	NA	88,38
c1908	25	53	3.03	68	4.65	96,50	93,05	99,64	96,29	88,68
c2670	140	160	1.40	179	2.72	93,90	93,37	98,93	98,35	88,04
c3540	22	56	1.90	95	4.09	93,79	92,91	98,89	95,36	88,01
c5315	123	149	1.05	161	1.53	96,38	92,99	99,61	95,90	88,65
c6288	32	49	0.58	64	1.10	84,14	92,73	93,25	93,93	82,99
c7552	108	134	0.69	158	1.32	96,22	92,86	99,58	94,85	88,62
b02	5	8	8.15	9	10.87	93,28	93,95	98,70	NA	87,84
b03	34	43	4.25	47	6.14	96,75	93,88	99,68	NA	88,72
b04	74	99	3.23	109	4.52%	95,53	92,44	99,41	98,79	88,48
b05	60	73	1.08	91	2.57	93,30	93,06	98,71	96,41	87,85
b06	15	22	8.64	26	13.58	96,26	94,30	99,59	NA	88,63
b07	57	80	4.58	84	5.38	94,11	92,59	99,00	99,66	88,11
b09	29	40	4.96	44	6.77	97,13	93,75	99,75	NA	88,78
b10	23	36	5.28	50	10.97	97,34	94,73	99,79	NA	88,81
b11	37	76	6.14	94	8.97	93,91	93,40	98,93	98,77	88,04
b12	127	139	0.85	167	2.84	97,79	93,37	99,85	98,05	88,87
b13	63	66	0.67	70	1.56	97,83	93,54	99,86	99,40	88,88

5. CONCLUSION

This paper analyzes the behaviour of integrated circuits designed for test (DFT) and reliability (DFR) in presence of manufacturing defects and their ability to tolerate manufacturing

defects. The modified circuits into TMR structures provide a good compromise between manufacturing yield, reliability and area overhead. It is well known now, that the impact of the realization of fault-tolerant structure of the manufacturing yield and reliability can be positive when two conditions are respected (i) the manufacturing yield must be less than 1/AO, and (ii) the T probability must be greater than a value Tmin which depends on technological parameters of manufacture. But also the optimization of fault tolerance through a judicious choice of the partitioning, and key locations within the circuit would be more appropriate to vote. However, redundancy consumes more energy and increases the propagation time through the circuits. We must therefore analyze the interesting compromise including assessing system-level redundancy to what percentage it is possible to go not to lose the benefits expected for new technologies.

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