Effect of Mobility and Velocity Saturation on Drain Current of Silicon N-MOSFET

A. S. M. Bakibillah,[a] Md. Nazibur Rahman[b]
[a, b] Department of Electrical & Electronic Engineering, American International University Bangladesh (AIUB), Dhaka 1213, Bangladesh
bakibillah@aiub.edu, nrahman.30@gmail.com

Abstract. In this paper, drain current as a function of mobility and velocity saturation is investigated individually at room temperature and I_d-V_{ds} characteristics curves are analyzed at threshold voltage (V_{gs}) of 0.73V for short channel Silicon n-MOS. For characterization, n-MOS model N08 is chosen which has specific mobility (μ_n) of 424.9 cm^2/Vs and saturation velocity (v_{sat}) of 9.127×104 cm/s. The simulation is accomplished using LTSPICE and the data is analyzed and characterized using MatLab. A good agreement between the model and the measured data is obtained. For both cases it is found that the drain current increases significantly with the increase in mobility and saturation velocity.

Keywords: Mobility, velocity saturation, drain current, MOSFET.

1 INTRODUCTION

The mobility and saturation velocity are two important model parameters that have significant contributions on modeling and characterization of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Mobility in MOSFET can be characterized by how quickly an electron can move through the channel when pulled by an electric field. However it is critical to find a good mobility model for the accurate modeling of MOSFET because scattering mechanisms responsible for surface mobility basically include photons, surface roughness and coulombic scattering that have certain amount of uncertainty (Cheng & Sullivan, 1974). Also, temperature dependence of mobility is a key factor for the MOSFET temperature behavior (Wolpert & Ampadu, 2012). For good quality interfaces (smooth and uniform), the dominant scattering mechanism is due to photon scattering at room temperature. In general sense, variation of mobility depends upon several process parameters and bias conditions. For example, mobility depends on substrate doping concentration, gate oxide thickness, gate and substrate voltages, threshold voltage etc. (Dunga et al., 2006). Also with device scaling, increasing doping concentration for adjusting threshold voltage causes random dopant fluctuations and degrades the channel mobility (Hariharan, Vasi & Rao, 2008). On the other hand, velocity saturation in MOSFET is a phenomenon which occurs due to high electric field that causes the drift velocity to reach a maximum value as with the degradation of mobility (Peng & Ismail, 2007). The saturation in MOSFET means that the change in V_{ds} will not produce significant change in the drain current (I_d) i.e. the current through the device will be almost constant. This is also called pinch off to indicate the lack of channel region near the drain. The occurrence of saturation at a particular electric field varies with different semiconductors and also critical electric field E_c has an effect on v_{sat} (Sodini, Ko & Moll, 1984; Gildenblat et al., 2006). In nanoelectronic devices, the high electric fields up to 10^6 V/cm increase scattering rate of highly energetic electrons with the average carrier energy which reduces the transconductance in the saturation mode (Peng & Ismail, 2007; Arora, 2000). In this work the effect of change in mobility and saturation velocity is shown on drain current for short channel operation of n-MOSFET.

2 DEVICE MODELING

In the necessity to obtain higher performance regarding speed, functionality and chip density, the channel length (L) and channel width (W) are being down scaled (Sakurai & Newton, 1991). But as the device scaling makes the channel length less than a micron (L < 1μ), second order effects that were ignored for long channel devices become prominent which includes velocity saturation, threshold voltage variations, hot carrier effects and so on (Taur et al., 1997). The basic structure of a Silicon n-channel MOSFET is shown in Fig. 1.

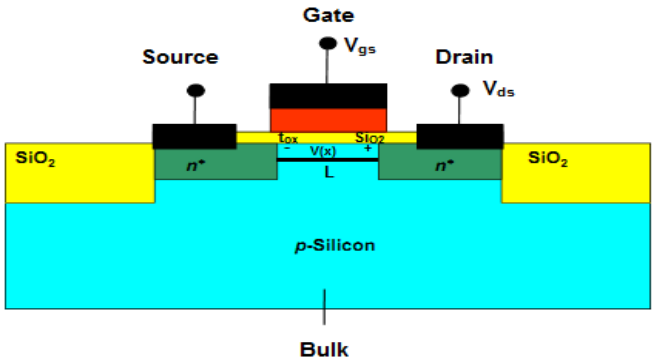

Fig. 1: Basic structure of an N-MOS

In the performance of a MOSFET, the effective mobility of inversion layer carriers is a significant factor [5]. When V_{gs} and V_{ds} are applied, the induced channel charge at $V(x)$ is

$$Q_i(x) = -WC_{ox}[V_{gs} - V(x) - V_{th}]. \quad (1)$$

The current is given as a product of the drift velocity of the carriers v_n and the available charge as

$$I_d = V_n Q_i(x) = -WC_{ox}[V_{gs} - V(x) - V_{th}]v_n. \quad (2)$$

The mobility of electrons is normally twice than that of holes. The electron velocity is related to the electric field through the mobility as

$$v_n = -\mu_n E(x) = -\mu_n \frac{dV(x)}{dx}. \quad (3)$$

Combining Eqs. (1) and (3) in (2), gives

$$I_d d(x) = \mu_n WC_{ox}[V_{gs} - V(x) - V_{th}]dV. \quad (4)$$

Integrating Eq. (4) from 0 to L gives the drain current of the transistor,

$$\int_0^L I_d d(x) = \int_{V=0}^{V=V_{ds}} \mu_n WC_{ox}[V_{gs} - V(x) - V_{th}]dV, \quad (5)$$

$$I_d = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right]. \quad (6)$$

When increasingV_{ds}, the electric field reaches a critical value E_c and the velocity of the carriers tends to saturate which is defined as (Assaderaghi, Ko & Hu, 1993)

$$E(x) = E_c = \frac{v_{sat}}{\mu_n}. \quad (7)$$

Now from Eq. (4), with $\mu_n dV = v_{sat}$ the drain current becomes,

$$I_{dsat} = v_{sat} C_{ox} W\left(V_{gs} - V_{th} - V_{dsat}\right). \quad (8)$$

This model describes the drain current as a function of mobility and velocity saturation.

3 RESULTS AND DISCUSSION

From the derived mathematical model it is clear that mobility and velocity saturation have certain effects on drain current. The typical values of mobility and velocity saturation for this n-MOS transistor are 424.9 cm^2/Vs and 9.127×10^4 cm/s respectively. To observe the effect on drain current the mobility and velocity saturation of transistor M2 are increased and decreased by ± 10% (at Temp = Tnom) and the simulation is performed using LTSPICE. The simulation data is then plotted and characterized using MatLab. The simulation model of mobility and velocity saturation for short channel n-MOS and I_d-V_{ds} characteristics curves are shown in Fig. 2 and Fig. 3 respectively.

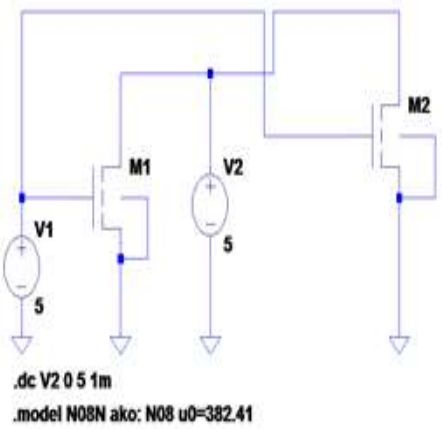

Fig. 2(a): Mobility decreased by 10%

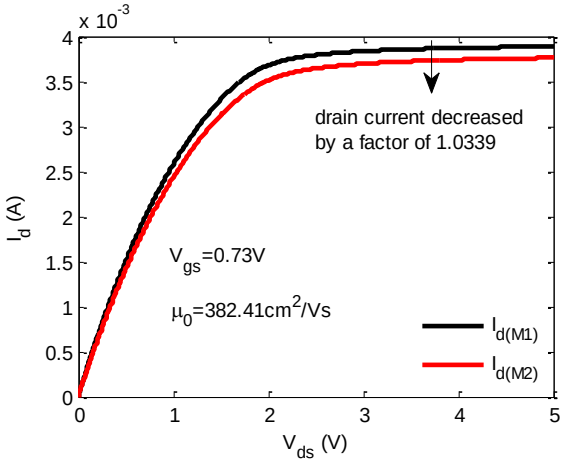

Fig. 2(b): I_d-V_{ds} characteristics curves showing the effect of decreased mobility on drain current at room temperature for short channel operation. The drain current reduced by a factor of 1.0339.

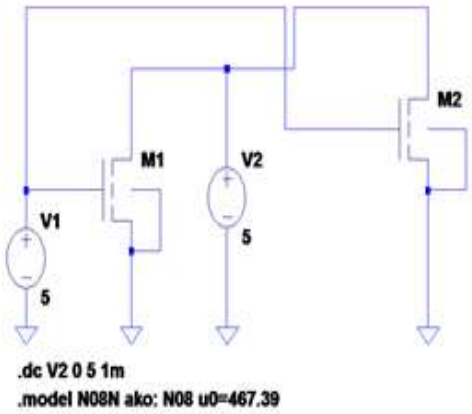

Fig. 2(c): Mobility increased by 10%

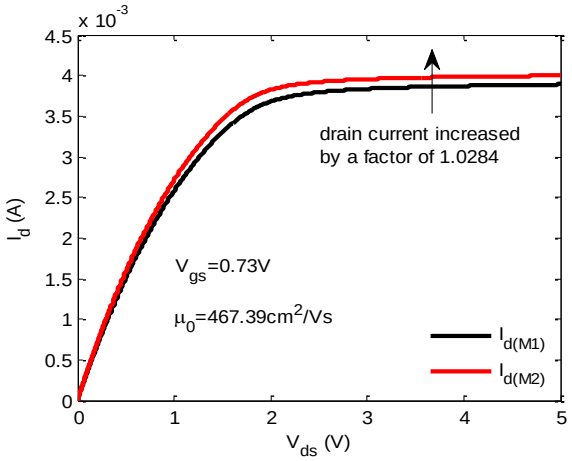

Fig. 2(d): I_d-V_{ds} characteristics curves showing the effect of increased mobility on drain current at room temperature for short channel operation. The drain current enhanced by a factor of 1.0284.

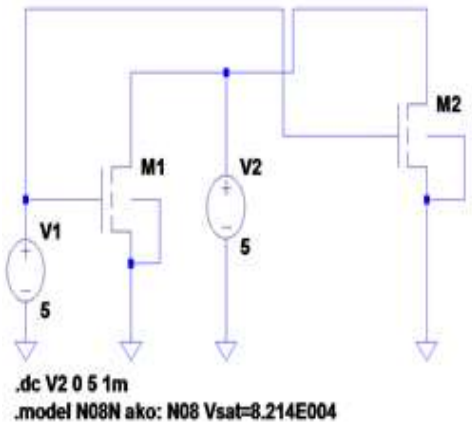

Fig. 3(a): V_{sat} decreased by 10%

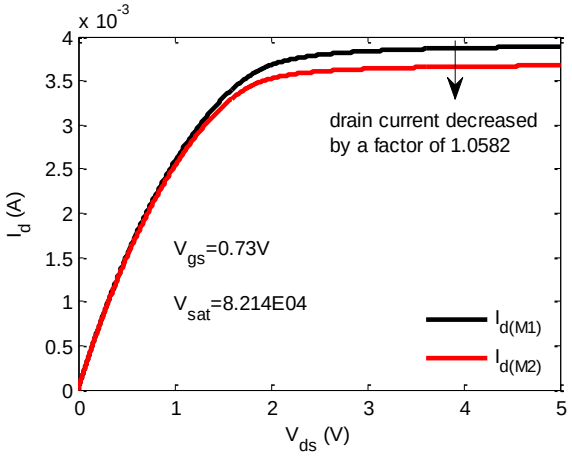

Fig. 3(b): I_d-V_{ds} characteristics curves showing the effect of reduced velocity saturation on drain current at room temperature for short channel operation. The drain current decreased by a factor of 1.0582.

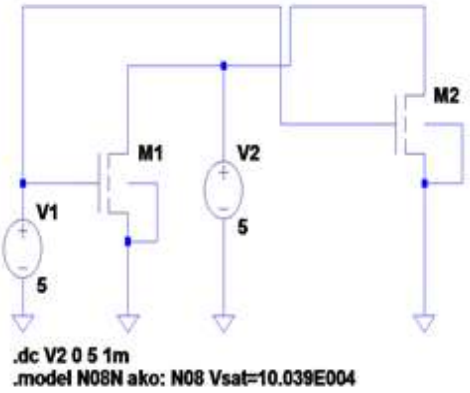

Fig. 3(c): V_{sat} increased by 10%

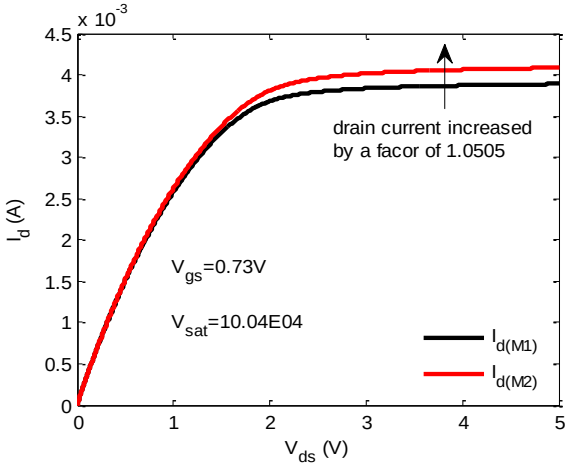

Fig. 3(c): I_d-V_{ds} characteristics curves showing the effect of increased velocity saturation on drain current at room temperature for short channel operation. The drain current enhanced by a factor of 1.0505.

Form the above figures; it is evident that mobility and velocity saturation have significant effects on drain current. But velocity saturation has slightly dominant effect on drain current compared to mobility for short channel operation at room temperature.

4 CONCLUSION

This paper investigates the effect of mobility and velocity saturation on drain current at room temperature for silicon n-MOSFET. The simulation results obtained in this work are compatible with analytical model of short channel Si n-MOS. In order to scale MOSFET devices these effects have to be considered. However, in order to accurately simulate the transistor behavior, complex formulas have to be used to describe the current under all operating conditions. Over the years, several elaborate models are developed which include the parasitic elements (diodes, resistors, etc.) in a closed form. The further investigation can be done for III-V n-MOSFETS over wide range of temperature variations.

References

Cheng, Y.C., & Sullivan, E.A. (1974). Effect of Coulombic Scattering on Silicon Surface Mobility. *J. Appl. Phys.*, 45, pp. 187-192. DOI: 10.1063/1.1662957

Wolpert, David Wolpert, & Ampadu, Paul. (2012). Managing Temperature Effects in Nanoscale Adaptive Systems. *Springer*, XXII, 174. DOI: 10.1007/978-1-4614-0748-5

Dunga, Mohan V., Xi, Xuemei (Jane), He, Jin, Liu, Weidong, Cao, Kanyu M., Jin, Xiaodong, Ou, Jeff J., & Chan, Mansun. (2006). *BSIM4.6.0 MOSFET Model.* User's Manual, University of California, Berkeley.

Hariharan, Venkatnarayan, Vasi, Juzer, & Rao, V. Ramgopal. (2008). Drain Current Model Including Velocity Saturation for Symmetric Double-Gate MOSFET. *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2173–2180. DOI: 10.1109/TED.2008.926745

Peng, Michael Tan Loong, & Ismail, Razali. (2007). Modeling of Nanoscale MOSFET Performance in the Velocity Saturation Region. *ELEKTRIKA*, vol. 9, no. 1, pp. 37-41

Sodini, C. G., Ko, P.-K., & Moll, J. L. (1984). The effect of high fields on MOS device and circuit performance. *IEEE Trans. Electron Devices*, vol. ED-31, no. 10, pp. 1386–139. DOI: 10.1109/T-ED.1984.21721

Gildenblat, G., Li, X., Wu, W., Wang, H., Jha, A., Langevelde, R. van, Smit, G. D. J., Scholten, A. J., & Klaassen, D. B. M. (2006). PSP: An advanced surface-potential-based MOSFET model for circuit simulation. *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1979–1993. DOI: 10.1109/TED.2005.881006

Arora, V. K. (2000). High-Field Effects in Sub-Micron Devices. *Conference on Optoelectronic and Microelectronic Materials and Devices*, pp. 33-40. DOI: 10.1109/COMMAD.2000.1022886

Sakurai, T. & Newton, A. R. (1991). A simple MOSFET model for circuit analysis. *IEEE Trans. Electron Devices*, vol. 38, no. 4, pp. 887-894. DOI: 10.1109/16.75219

Taur, Y., Buchanan, D. A., Chen, W., Frank, D. J., Ismail, K. E., Lo, S.-H., Sai-Halasz, G. A., Viswanathan, R. G., Wann, H.-J. C., Wind, S. J., & Wong, H.-S. (1997). CMOS Scaling into the Nanometer Regime. *Proceedings of the IEEE*, vol. 85, no. 4, pp. 486–504. DOI: 10.1109/5.573737

Assaderaghi, F., Ko, P. K., & Hu, C. (1993). Observation of velocity overshoot in silicon inversion layers. *IEEE Electron Device Letters*, vol. 14, no. 10, pp. 484-86. DOI: 10.1109/55.244738